EE6324: FINAL PROJECT

Team Member 1: Vallabh Ramakanth (EE17B068)

Team Member 2: Aditya Sundararajan (EE17B102)

Objective: To design a phase-locked loop operating at 2.56GHz with a reference clock of 40MHz

PLL Architecture:

A type II order 3 Phase-Locked Loop was designed to meet the required specifications. A type II PLL is required to ensure that the loop will lock to zero phase error for a step change in frequency while a 3rd order loop will ensure stability.
A phase margin of 60° was targeted to ensure that the loop is stable with minimal ringing. The Unity Gain Frequency (UGB) was chosen to be 0.1*Wref. This is because the VCO was already designed and its phase noise was characterized. This phase noise of the VCO was found to be much larger than the noise contribution of any of the other blocks (for reasonable values of Gm and R). A larger unity gain frequency will result in suppression of the VCO noise since the Noise Transfer Function for the VCO is high pass in nature and can thus cut off more noise. We cannot use a unity gain frequency larger than 0.1*Wref as our continuous time model may not be valid then. The plot of noise contributions of various blocks is attached later under the Phase Noise section.

Reference Spurs will be minimized by minimizing the mismatch in the charge pump current sources and choosing the right value of C2 in the loop filter (detailed later under Charge Pump Design). The last constraint enforced was that the slope of the phase plot of the PLL Loop Gain is zero at the unity gain frequency thus making it robust to process and mismatch variations.

However, hand calculations to ensure the right bandwidth and phase margin with minimal reference spurs (by using large C2) resulted in large values of capacitance. Thus, instead of the standard source switched charge pump architecture, the method of reducing current through C1 (by a factor α) to effectively "amplify" its capacitance was used. This is detailed in the Charge Pump section.
The transfer function of the Loop Filter and the overall loop gain of the PLL were now found to be:

$$\mathrm{LF}(s) = \frac{1 + sC_1R/\alpha}{\frac{sC_2^2}{\alpha(C_1+C_2)}\left(\frac{sC_1C_2R}{C_1+C_2}+1\right)}$$

$$\mathrm{LG}(s) = \frac{I_{cp}K_{vco}}{N}\frac{1 + sC_1R/\alpha}{\frac{s^2C_2^2}{\alpha(C_1+C_2)}\left(\frac{sC_1C_2R}{C_1+C_2}+1\right)}$$

The various component values of the PLL were then found to be:

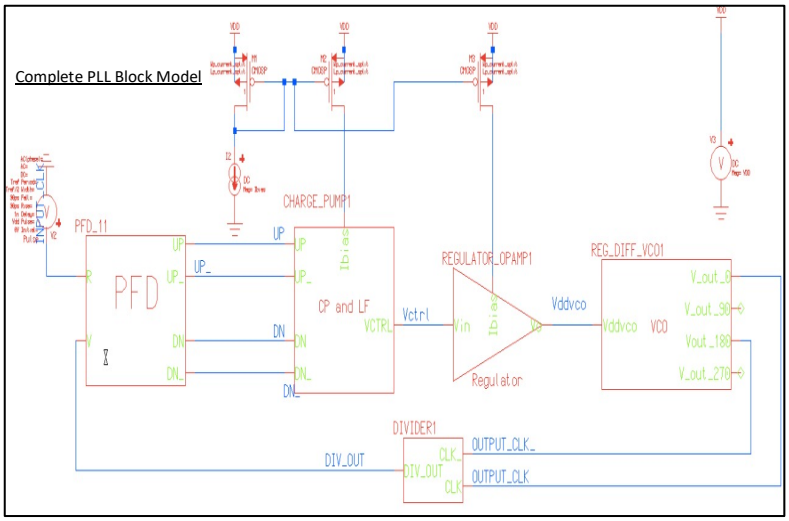
Charge Pump Current = 1mA

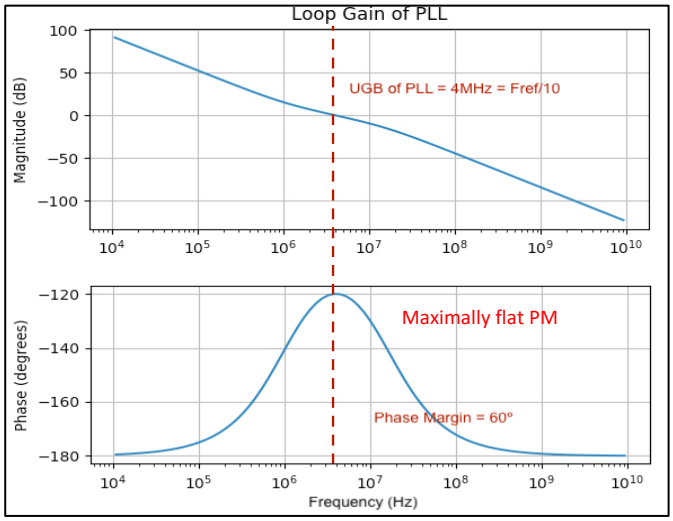
Loop Filter Resistor R = 5.9kΩ

Loop Filter Capacitor C1 = 2pF

Loop Filter Capacitor C2 = 17.7pF

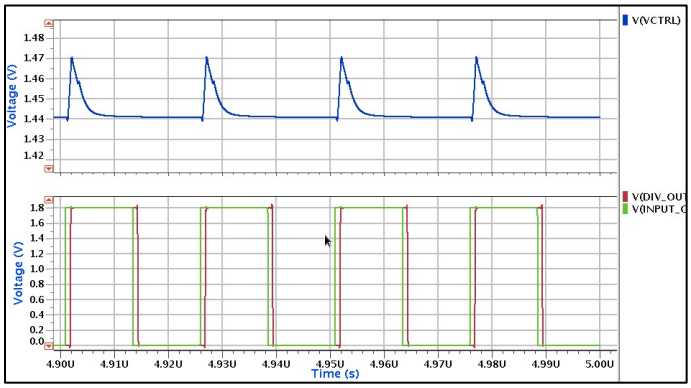
α = 0.08

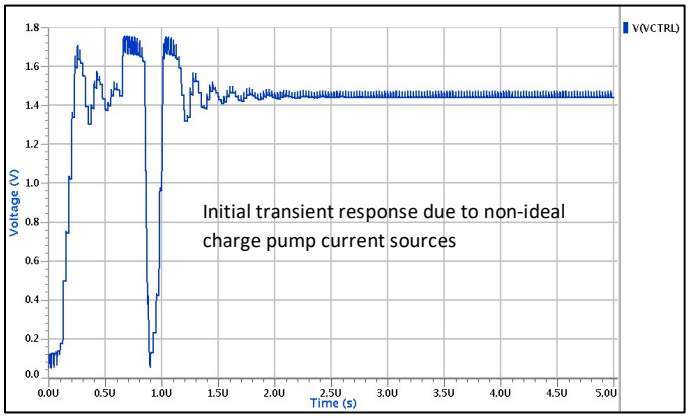




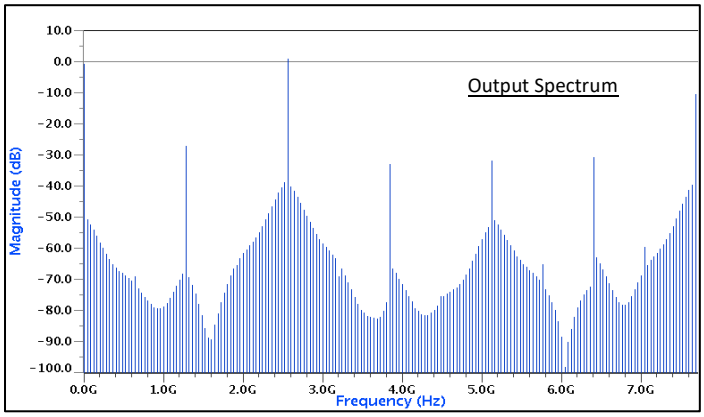
Final Performance and Specifications:

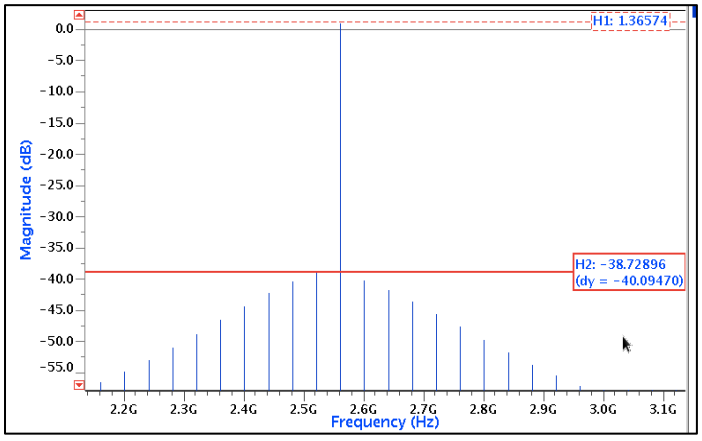
The PLL is able to successfully lock to the reference clock as seen below:



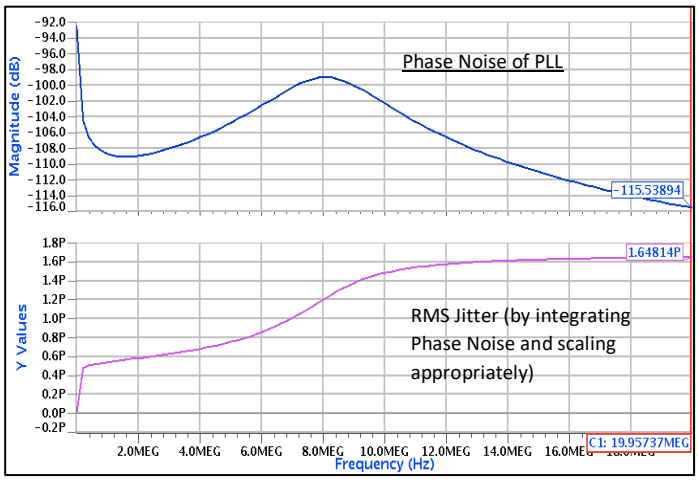


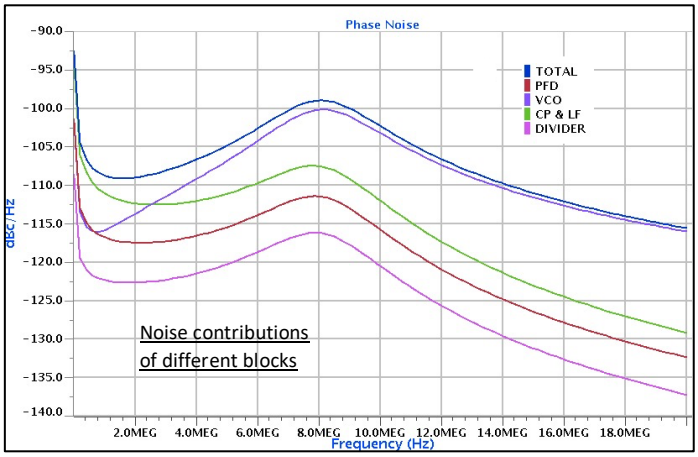
1. Operating Frequency and Reference Spurs: The required operating frequency of 2.56GHz was achieved with Reference Spurs < -40dBc as seen from the plot below. This was possible to minimization of mismatch between the charge pump current sources and the introduction of the switches in the loop filter to prevent discharge





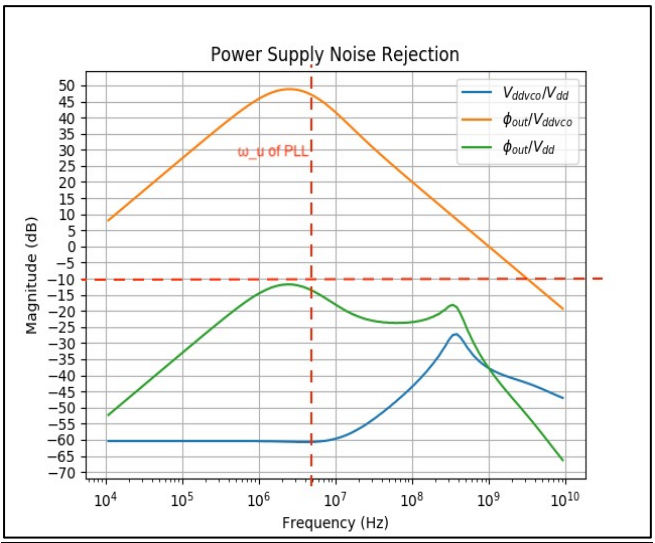
2. Jitter and Phase Noise: The plot of phase noise and jitter is seen below:

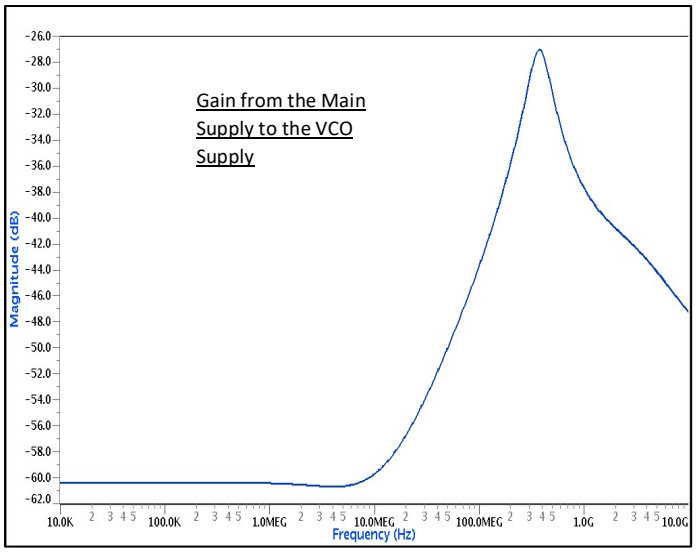




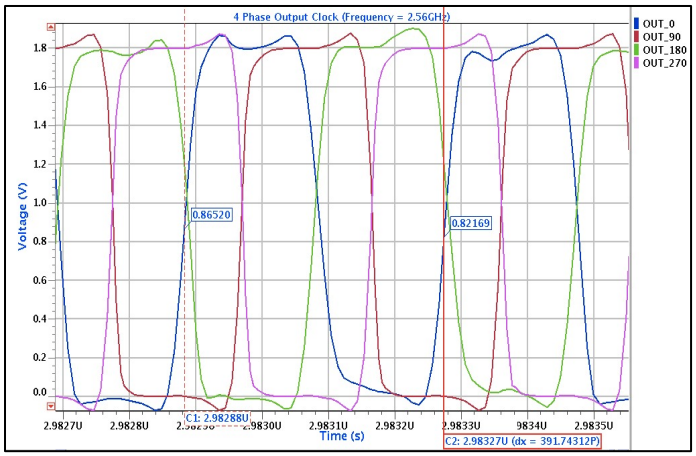
As we can see, the PLL has an RMS Jitter of 1.68ps which is less than 0.5% of the output clock period as required. We also see that the VCO noise dominates over the rest as expected. Thus, the choice of unity gain frequency is justified.

3. PSNR: The gain from the main supply to the supply of the VCO was simulated and then extracted to find the Power Supply Noise Rejection by modelling the rest of the PLL in Python. The final PSNR is less than 10dB as required

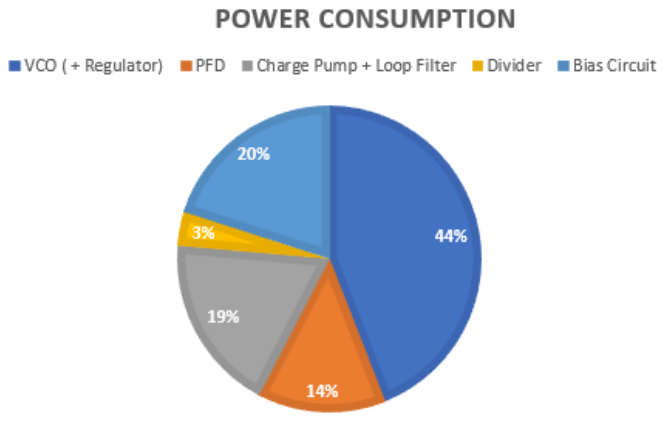




4. Output Phases: The PLL successfully generates output phase of 0, 90, 180 and 270 as seen below:

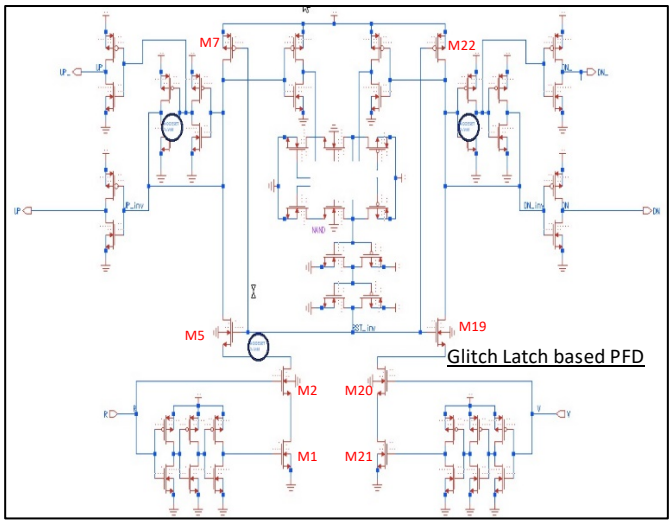


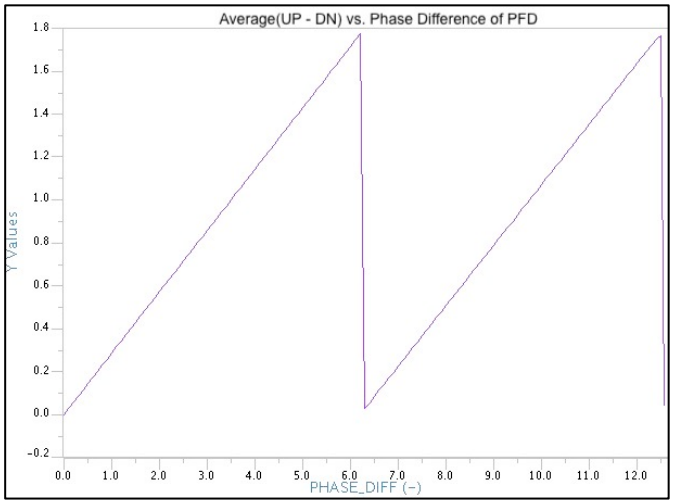
5. Power Consumption: The total power consumption of the system is 7.49mW at 1.8V supply. The various contributions are plotted in the Pie Chart below:



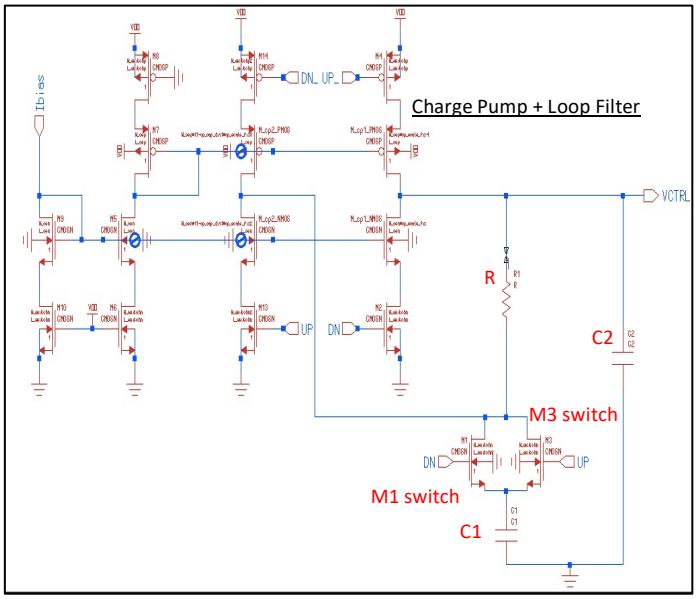
Design of Individual Blocks:

1. PFD: A glitch latch-based Phase -Frequency Detector was designed to decouple reset and overlap times and ensure that the PFD does not miss rising edges.

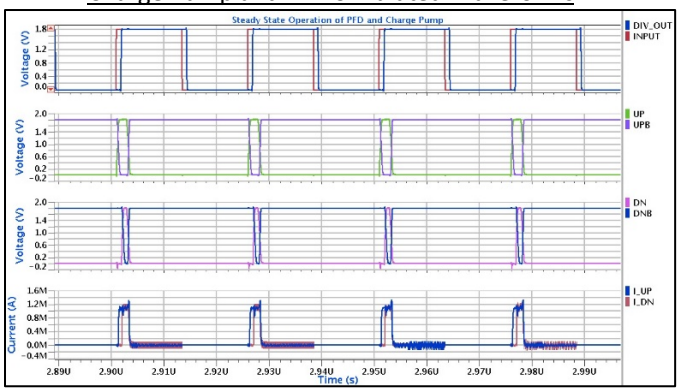




There is a small delay in the time taken to generated complementary outputs but this has been compensated for in the charge pump and loop filter as mentioned below. The gain of the PFD can be seen above to be 1/2pi as expected



Charge Pump and PFD Simulated Waveforms



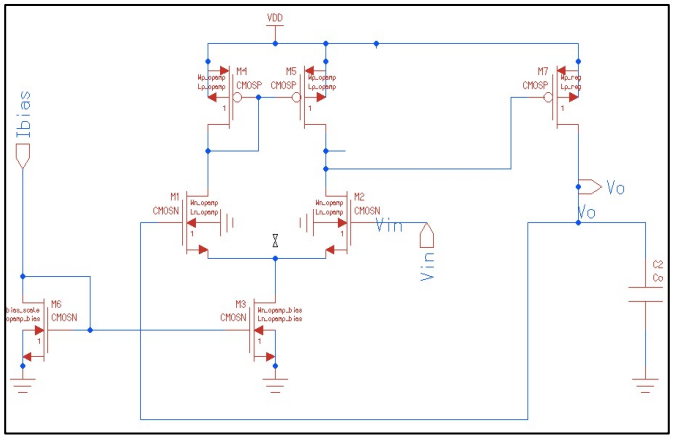
2. Charge Pump and Loop Filter:

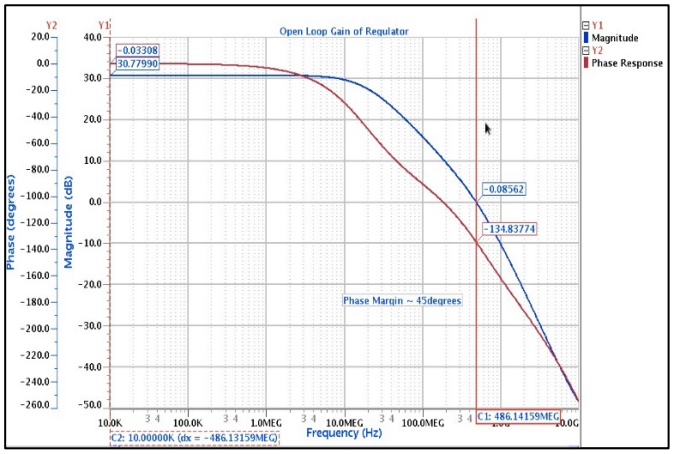
The Charge Pump as mentioned earlier was a source switched Charge Pump which reduces the current through C1 to effectively amplify its capacitance in the transfer function. The schematic is can be seen above
The initial design did not consist of the switches M1 and M3. However, it was found that the pole frequency was large enough that the capacitors C2 and C1 were discharging a significant amount within one reference period. This could be fixed by reducing the pole frequency which would worsen phase margin and the unity gain frequency (and thus noise).
Instead of compromising on this, **a novel design was explored where the switches M1 and M3 were added in series with C1 so that the loop filter capacitances cannot discharge when the charge pump currents are off**. This worked extremely well and was able to reduce the discharging and the reference spurs enough to meet the required specification.
Furthermore, the increased load on UP and DN now ensure that their delays are equal to those of their complements as required. The simulated waveform can be seen above. The variation of Vctrl was attached earlier. We can see that the charge pump currents are 1mA as required (from the main branch).

3. VCO:

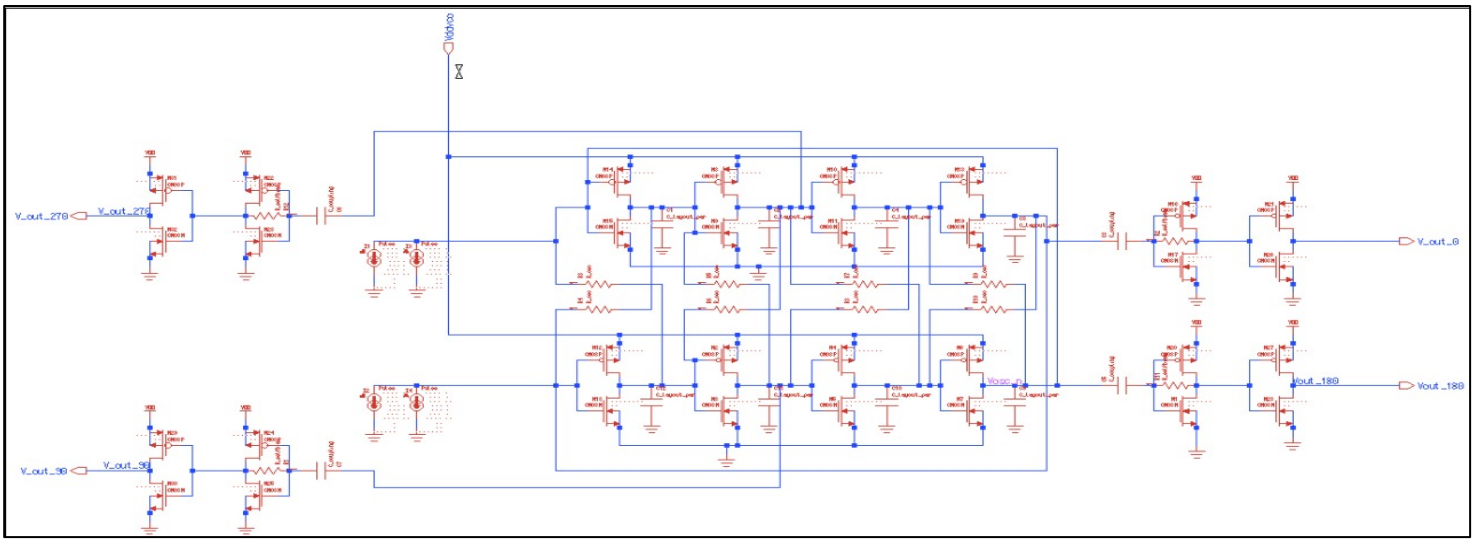
A pseudo differential supply regulated ring oscillator based VCO was designed to enable tuning of the output frequency. The schematic is as seen below (with parasitic capacitances added to model layout parasitics)

The supply regulator design is as follows:





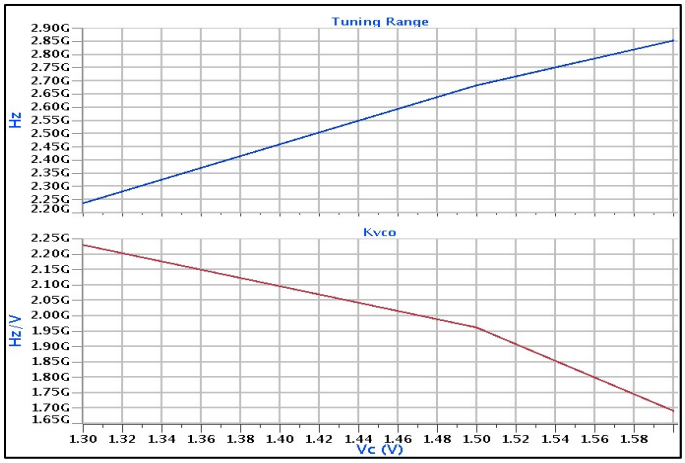
Where an NMOS input pair was used so that the gain from the supply to its output will be 1. This will effectively make the source-gate voltage of M7 close to zero and will suppress the supply noise. The loop was stabilised by making the supply node of the VCO as the dominant pole by increasing the capacitance at the node and making M7 small enough so that the opamp bandwidth is larger (while ensuring that it is in saturation). The loop gain of the regulator as seen above has a DC gain of 30dB with a phase margin of 45.

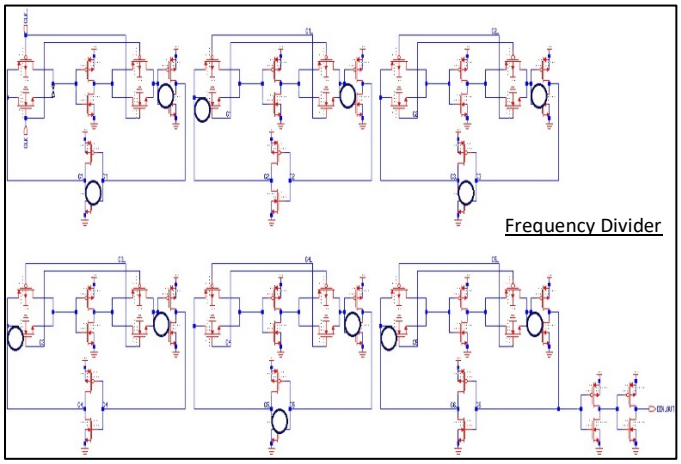


Ring Oscillator Based VCO

Here, there is a clear tradeoff between PM and gain from Vdd to Vdd,vco.

With this regulator the following plots for the tuning range and Kvco were obtained:





4. Frequency Divider:

A 6-bit counter was used to step down the frequency by 64. The schematic can be seen above and uses transmission gate-based D Flip Flops. Output buffers were also added to the divider to ensure that the divider is able to drive the PFD.

Summary and Conclusions:

The Phase-Locked Loop was successfully designed to meet the required specifications. This experience has given us an invaluable insight into the design of a complete system and all the various considerations and trade-offs that go into it.

To meet the given specifications, a system level design for first done to find the values of charge pump current and loop filter components. Since the VCO was already designed, Kvco and its noise was known too. On completion of the complete design of all the blocks it was found that there was significant deviation from the expected behaviour due to the charge pump and loop filter. Thus, extra switches were added in the loop filter to ensure that there is no discharging. Once this was done, the reference spurs were reduced heavily.

However, it should be noted that this might affect the continuous time transfer function of the PLL since the system has become more discrete now.

Noise analysis showed that the PLL was able to meet the required specification for jitter and had contributions from the various blocks as expected. We see that the total noise is dominated by the VCO and thus to reduce jitter even more, the VCO noise needs to be reduced.

Power Supply Noise was also sufficiently suppressed by the regulator opamp loop. However, to reduce it further a more sophisticated supply regulator can be used for the VCO like a multi-stage opamp.

Power consumption of the biasing circuit can be minimised further, however, it needs to be done carefully as it can also lead to amplification of noise.

Component Sizes:

PFD	
M7, M22	W=21u, L=0.18u
M1, M2, M5, M19, M20, M21	W=12.15u, L=0.18u
NMOS in NAND	W=0.27u, L=0.18u
PMOS in NAND	W=1.4u, L=0.18u
Inverter NMOS driving NAND	W=0.27u, L-0.18u
Inverter PMOS driving NAND	W=1.4u, L=0.18u
NAND to RST delay NMOS	W=0.27u, L=0.18u
NAND to RST delay PMOS	W=1.4u, L=0.18u
Cross coupled output inverter NMOS	W=0.81u, L=0.18u
Cross coupled output inverter PMOS	W=5.2u, L=0.18u
Other inverters NMOS	W=4.05u, L=0.18u
Other inverters PMOS	W=21u, L=0.18u
Charge Pump	
NMOS switch width	W=100u, L=0.18u
PMOS switch width	W=200u, L=0.18u
NMOS Current Source (into LF)	W=12.6u, L=0.18u
PMOS Current Source (into LF)	W=39u, L=0.18u
NMOS Current Source (out of LF)	W=7.54u, L=0.18u
PMOS Current Source (out of LF)	W=13.8u, L=0.18u
Bias circuits are half the size	
R	5.7kOhms
C1	2pF
C2	17.7pF
Regulator	
Tail NMOS	W=100u, L=0.36u
Biasing NMOS	W=25u, L=0.36u
NMOS input pair	W=100u, L=0.18u
PMOS Active Load	W=40u, L=0.18u
PMOS regulator	W=80u, L=0.36u
Co	20p
VCO	
Ring Oscillator inverter NMOS	W=1.08u, L=0.18u
Ring Oscillator inverter PMOS	W=5.6u, L=0.18u
R_osc (feedback resistors in RO)	4kOhms
Self-biased Buffer1 NMOS	0.27u, 0.18u
Self-biased Buffer1 PMOS	1.4u, 0.18u
Output Buffer NMOS	0.27u, 0.18u
Output Buffer PMOS	1.4u, 0.18u
$R_{selfbias}$, $C_{coupling}$	100kOhm, 0.5pF
Divider	
All NMOS (except output buffers) (1x)	0.27u, 0.18u
All PMOS (except output buffers) (1x)	1.4u, 0.18u
Output Buffer 1	4x unit size
Output Buffer 2	4x unit size

References:

1. *EE6324, Notes of course PLL, by Saurabh Saxena,* http://www.ee.iitm.ac.in/videolectures/doku.php?id=ee6324_2020